CLAIMS

What is claimed is:

1. A memory module comprising:

a detection device configured to produce an output signal having one of at least three voltage levels correlative to at least three respective selectable CAS latencies; and

a plurality of memory devices coupled to the detection device, wherein each of the plurality of memory devices comprises a single pin configured to receive the output signal and configured to set the CAS latency of the respective memory device correlative to the voltage levels of the output signal.

2. The memory module, as set forth in claim 1, wherein the detection device comprises a serial presence detect (SPD) device.

3. The memory module, as set forth in claim 1, wherein the memory module comprises a dual inline memory module (DIMM).

4. The memory module, as set forth in claim 1, wherein each of the plurality of memory devices comprises a synchronous dynamic random access memory (SDRAM) device.

5. The memory module, as set forth in claim 2, wherein the serial presence detect device comprises a writeable serial presence detect device configured to produce an output signal, the output signal being a multi-level voltage signal.

6. The memory module, as set forth in claim 5, wherein the multi-level voltage signal is in the range of -1.1 volts - +2.1 volts.

7. The memory module, as set forth in claim 5, wherein the multi-level voltage signal comprises one of eight voltage levels.

8. The memory module, as set forth in claim 7, wherein each of the eight voltage levels is separated by a voltage gap.

9. The memory module, as set forth in claim 7, wherein each of the plurality of memory devices comprises a sensing device coupled to the single pin and configured to sense the voltage level of the multi-level voltage signal and interpreting the corresponding CAS latency of the respective memory device, correlative to the voltage level of the voltage level.

10. A system comprising:

a processor; and

a plurality of memory modules operably coupled to the processor and wherein each of the plurality of memory modules comprises:

a detection device configured to produce an output signal having one of at least three voltage levels correlative to at least three respective selectable CAS latencies; and

a plurality of memory devices coupled to the detection device, wherein each of the plurality of memory devices comprises a single pin configured to receive the output signal and configured to set the CAS latency of the respective memory device, correlative to the voltage level of the output signal.

11. The system, as set forth in claim 10, wherein the detection device comprises a serial presence detect (SPD) device.

12. The system, as set forth in claim 10, wherein each of the plurality of memory modules comprises a dual inline memory module (DIMM).

13. The system, as set forth in claim 10, wherein each of the plurality of memory devices comprises a synchronous dynamic random access memory (SDRAM) device.

14. The system, as set forth in claim 10, wherein the serial presence detect device comprises a writeable serial presence detect device configured to produce an output signal, the output signal being a multi-level voltage signal.

15. The system, as set forth in claim 14, wherein the multi-level voltage signal is in the range of -1.1 volts - +2.1 volts.

16. The system, as set forth in claim 14, wherein the multi-level voltage signal comprises one of eight voltage levels.

17. The system, as set forth in claim 16, wherein each of the eight voltage levels is separated by a voltage gap.

18. The system, as set forth in claim 16, wherein each of the plurality of memory devices comprises a sensing device coupled to the single pin and configured to sense the voltage level of the multi-level voltage signal and interpret the corresponding CAS latency of the respective memory device, correlative to the voltage level of the voltage level.

19. A method of selecting a CAS latency in a system comprising a plurality of memory modules comprising the acts of:

sending a drive signal to a static pin on a memory device, wherein the drive signal comprises one of at least three voltage levels;

assigning one of at least three corresponding CAS latencies, wherein the corresponding CAS latency is dependent on the voltage level of the drive signal.

20. The method, as set forth in claim 19, wherein the act of sending a drive signal comprises the act of sending the drive signal from a serial presence detect (SPD) device.

21. The method, as set forth in claim 20, comprising the act of sending a CAS latency select signal to the serial presence detect device, wherein the CAS latency select signal corresponds to the lowest CAS latency achievable by all of the memory modules in the system.

22. The method, as set forth in claim 21, comprising the act of reading a configuration device on a memory module to determine the CAS latencies that may be selected for the memory module.

23. The method, as set forth in claim 22, wherein the act of reading a configuration device comprises the act of reading the serial presence detect (SPD) device to determine the CAS latencies that may be selected for the memory module.

24. The method, as set forth in claim 23, wherein the act of reading a device comprises the act of reading the device at system boot-up.

25. The method, as set forth in claim 19, wherein the act of assigning a corresponding CAS latency, comprises the acts of :

sensing the voltage level of the drive signal; and

converting the drive signal into the corresponding CAS latency.

26. The method, as set forth in claim 25, comprising the act of checking a register to determine the CAS latency which corresponds to the current voltage level of the drive signal.

27. A method of manufacturing a memory device comprising the act of producing a memory device having a single static pin coupled to a sensing device, wherein the sensing device is adapted to receive at least three different voltage levels and select from at least three different CAS latencies correlative to the voltage level.